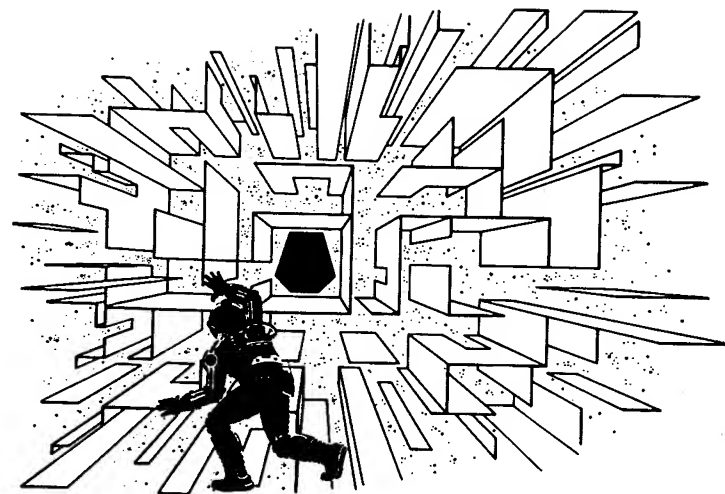


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## NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.

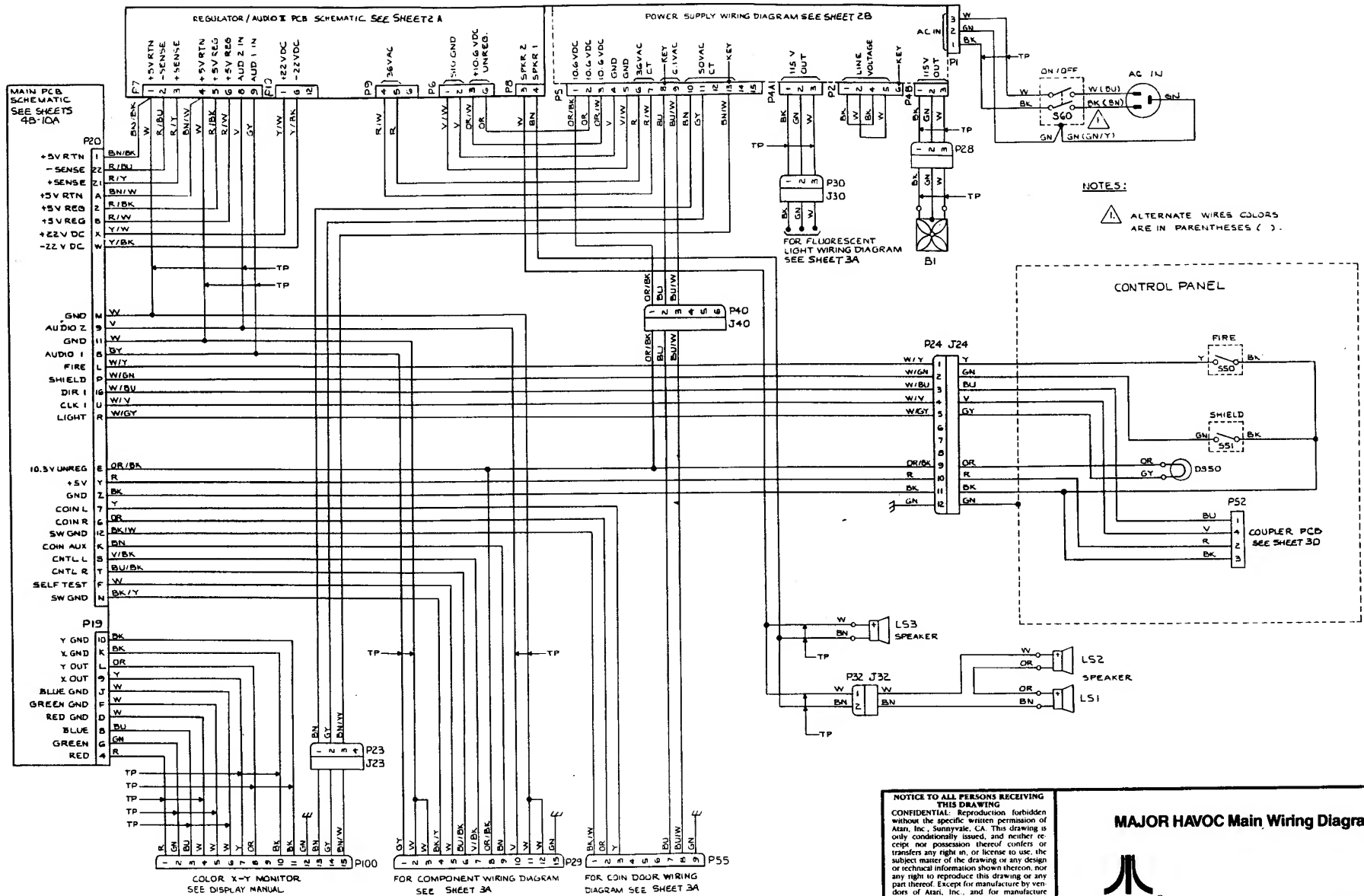


## Schematic Package Supplement to

The Adventures of  
**MAJOR HAVOC**

## Operators Manual





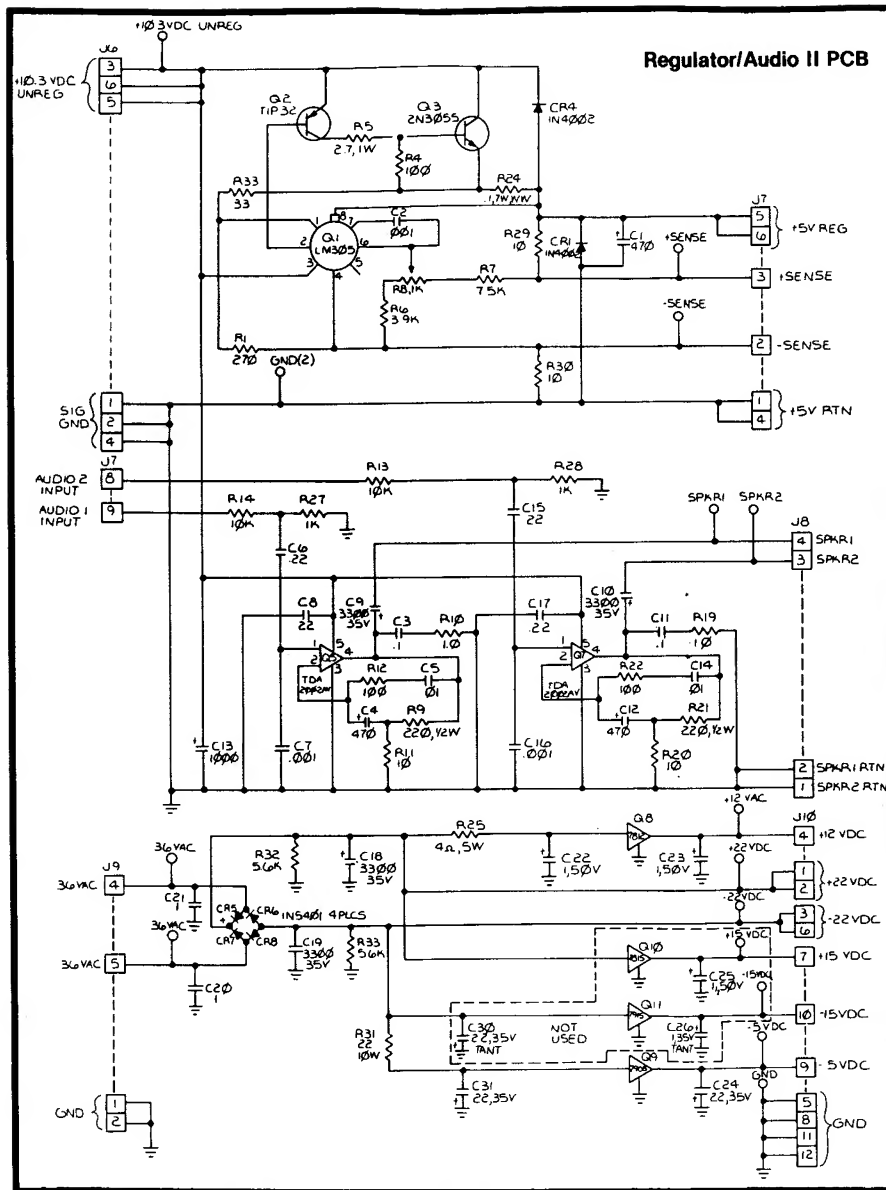
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# MAJOR HAVOC Main Wiring Diagram



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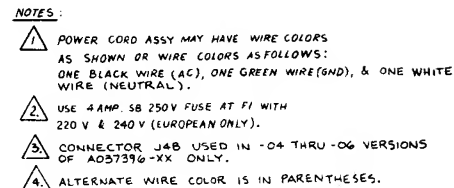
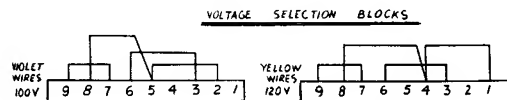
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## MAJOR HAVOC Regulator/Audio II PCB Schematic Diagram



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### MAJOR HAVOC Color X-Y Power Supply Wiring Diagram

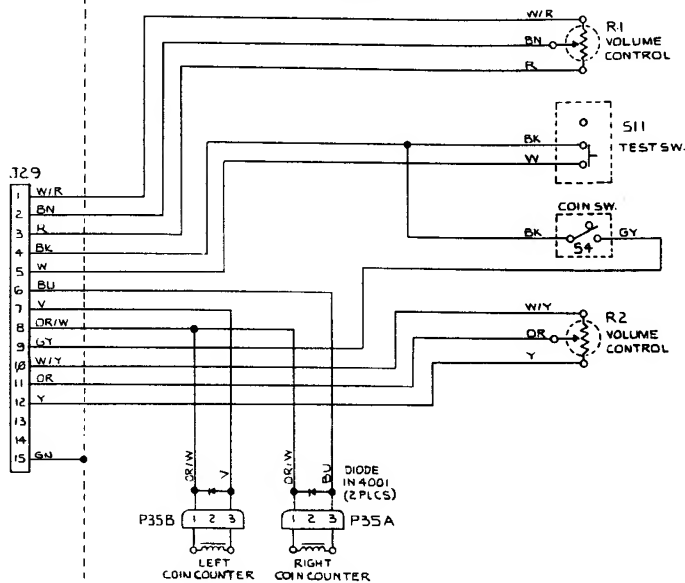


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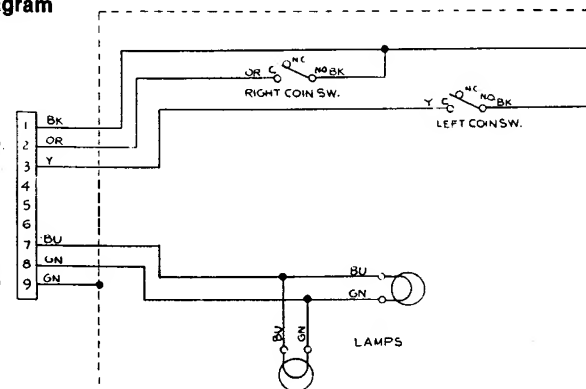
# Utility Panel Wiring Diagram

## WIRING DIAGRAM

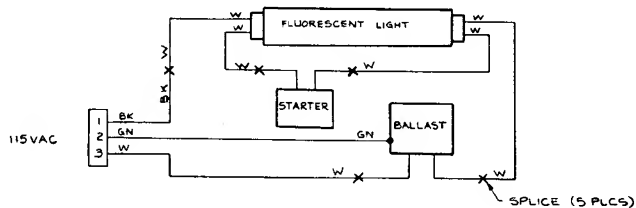


# Coin Door Wiring Diagram

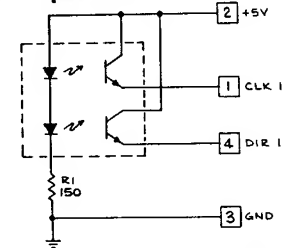
SW GND  
RIGHT COIN SW.  
LEFT COIN SW.  
  
+10VDC  
G 3 VAC  
G 3 VAC  
CHASSIS GND



# Fluorescent Light Wiring Diagram



# Coupler PCB



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# MAJOR HAVOC Game Interfaces



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## Major Havoc Memory Map Alpha (α) Microprocessor

HEXA- DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES																READ/ WRITE	DATA BUS SIGNAL LINES								FUNCTION
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
0000-01FF	0	0	0	0	0	0	0	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	PROGRAM RAM (1/2K)
0200-07FF	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	PAGED PROGRAM RAM (3K)
0800-09FF	0	0	0	0	1	0	0	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	PROGRAM RAM (1/2K)
1000	0	0	0	1	0	0	0										R	D	D	D	D	D	D	D	D	GAMMA COMM. READ PORT
1200	0	0	0	1	0	0	1										R	D								RIGHT COIN SW. (PLAYER 1=0)
1200	0	0	0	1	0	0	1										R	D								LEFT COIN SW. (PLAYER 1=0)
1200	0	0	0	1	0	0	1										R		D							AUX. COIN SW. (PLAYER 1=0)
1200	0	0	0	1	0	0	1										R	D								SELFTEST (PLAYER 1=1)
1200	0	0	0	1	0	0	1										R		D							CABINET SW. (PLAYER 1=1)
1200	0	0	0	1	0	0	1										R			D						AUX. COIN SW. (PLAYER 1=1)
1200	0	0	0	1	0	0	1										R					D				GAMMA RCVD FLAG
1200	0	0	0	1	0	0	1										R						D			GAMMA XMTD FLAG
1200	0	0	0	1	0	0	1										R							D		2.4KHz
1200	0	0	0	1	0	0	1										R							D		VEC. GEN. HALT FLAG
1400-141F	0	0	0	1	0	1	0						A	A	A	A	W					D	D	D	D	COLORAM
1600	0	0	0	1	0	1	1	0	0	0							W	D								INVERT Y
1600	0	0	0	1	0	1	1	0	0	0							W	D	D							INVERT X
1600	0	0	0	1	0	1	1	0	0	0							W		D							PLAYER 1
1600	0	0	0	1	0	1	1	0	0	0							W				D					GAMMA RESET
1600	0	0	0	1	0	1	1	0	0	0							W						D			ROLLER CONTROL LIGHT
1640	0	0	0	1	0	1	1	0	0	1							W									VEC. GEN. GO
1680	0	0	0	1	0	1	1	0	1	0							W									WATCHDOG CLEAR
16C0	0	0	0	1	0	1	1	0	1	1							W									VEC. GEN. RESET
1700	0	0	0	1	0	1	1	1	0	0							W									IRQ ACKNOWLEDGE
1740	0	0	0	1	0	1	1	1	0	1							W									PROGRAM ROM MMU
1780	0	0	0	1	0	1	1	1	1	0							W									PROGRAM RAM SELECT
17C0	0	0	0	1	0	1	1	1	1	1							W									GAMMA COMM. WRITE PORT
2000-3FFF	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	PAGED PROG. ROM (32K)
4000-4FFF	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	VEC. GEN. RAM (4K)
5000-5FFF	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	VEC. GEN. ROM (4K)
6000-7FFF	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	PAGED VEC. GEN. ROM (32K)
8000-FFFF	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	PROGRAM ROM (32K)

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### MAJOR HAVOC Memory Map Alpha (α) Microprocessor



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## Major Havoc Memory Map Gamma (γ) Microprocessor

HEXA- DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES																READ/ WRITE	DATA BUS SIGNAL LINES								FUNCTION
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
0000-07FF	0	0	0			A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	PROGRAM RAM (2K)
2000-203F	0	0	1	0	0						A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	QUAD. CUSTOM I/O
2800	0	0	1	0	1												R	D								FIRE 1 SWITCH
2800	0	0	1	0	1												R		D							SHIELD 1 SWITCH
2800	0	0	1	0	1												R			D						FIRE 2 SWITCH
2800	0	0	1	0	1												R				D					SHIELD 2 SWITCH
2800	0	0	1	0	1												R						D			ALPHA RCVD FLAG
2800	0	0	1	0	1												R							D		ALPHA XMTD FLAG
3000	0	0	1	1	0												R	D	D	D	D	D	D	D	D	ALPHA COMM. READ PORT
3800-3803	0	0	1	1	1										A	A	R	D	D	D	D	D	D	D	D	ROLLER CONTROL INPUT
4000	0	1	0	0	0												W									IRQ ACKNOWLEDGE
4800	0	1	0	0	1												W							D		LEFT COIN COUNTER
4800	0	1	0	0	1												W							D		RIGHT COIN COUNTER
5000	0	1	0	1	0																			D		ALPHA COMM. WRITE PORT
6000-61FF	0	1	1					A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	EEROM
8000-BFFF	1		A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	PROGRAM ROM

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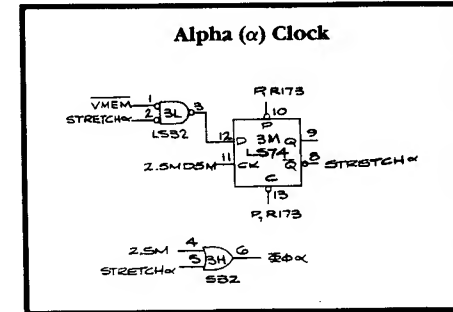
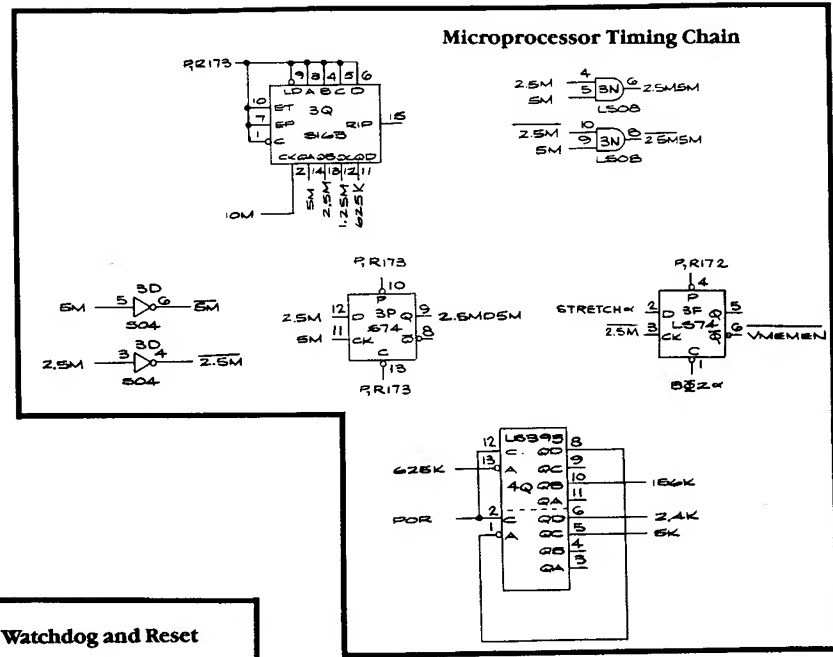
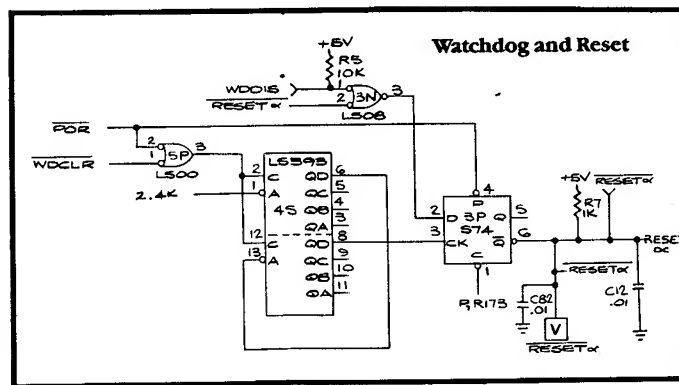
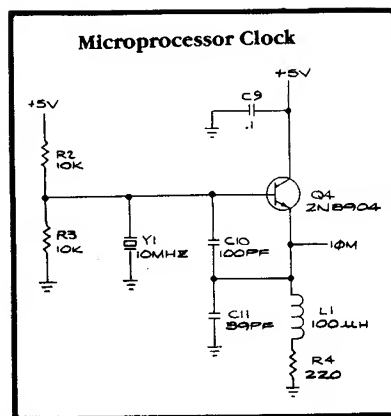
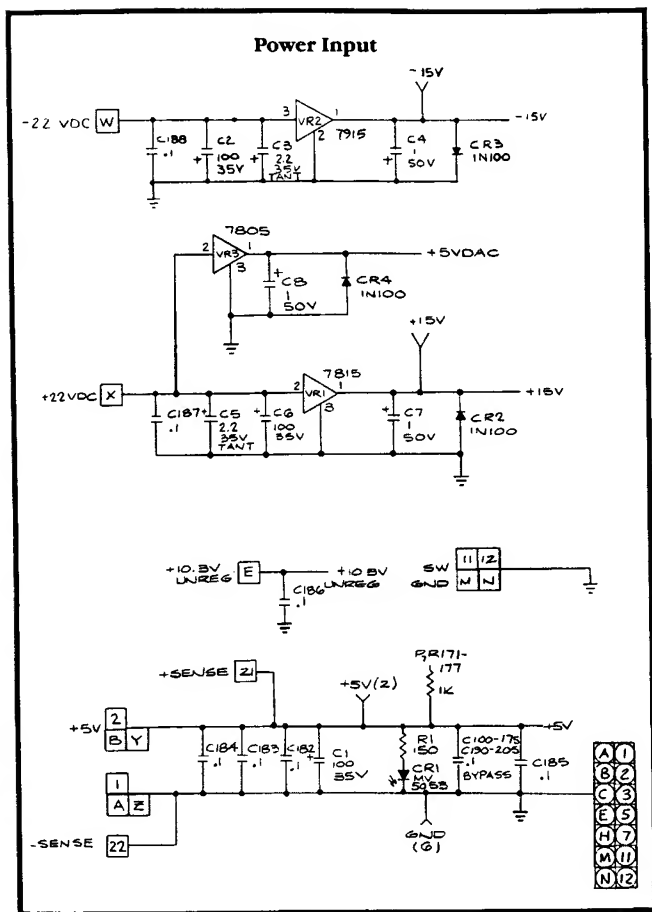
### MAJOR HAVOC Memory Map Gamma (γ) Microprocessor



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**MAJOR HAVOC Main PCB Schematic Diagram**

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### Power-Up Reset

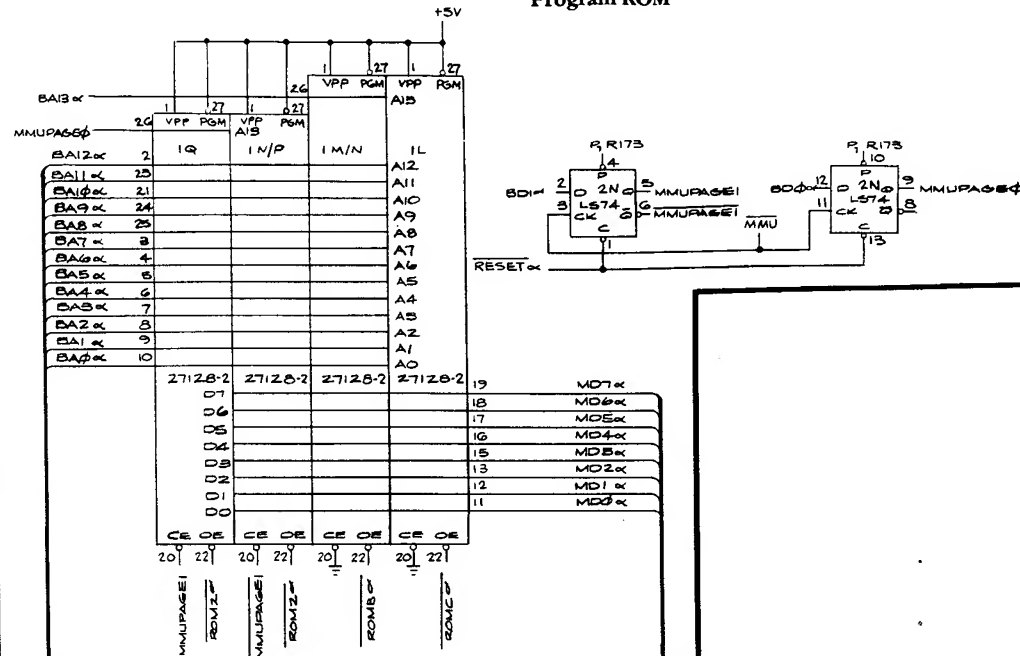
The diagram illustrates a power-up reset circuit. It begins with a voltage divider consisting of resistors R20 (5.6K) and R21 (10K) connected to a +10.5V supply. The midpoint of this divider is connected to the non-inverting input (pin 3) of an LM324 op-amp. The op-amp's inverting input (pin 2) is connected to a +5V supply. The op-amp is configured with its output (pin 1) to its inverting input (pin 2) and its non-inverting input (pin 3) to ground. The output of the op-amp (pin 1) is connected to the input (pin 1B) of a 74LS04 inverter. The output of this inverter (pin 12) is connected to the input (pin 3) of a second 74LS04 inverter. The output of the second inverter (pin 4) is connected to a pull-up resistor (POR) and the +5V supply. A CR5 capacitor (1000) is connected between the +5V supply and the input of the first 74LS04 inverter. A RESET signal is shown connected to the input of the first 74LS04 inverter.

### MAJOR HAVOC Main PCB Schematic Diagram

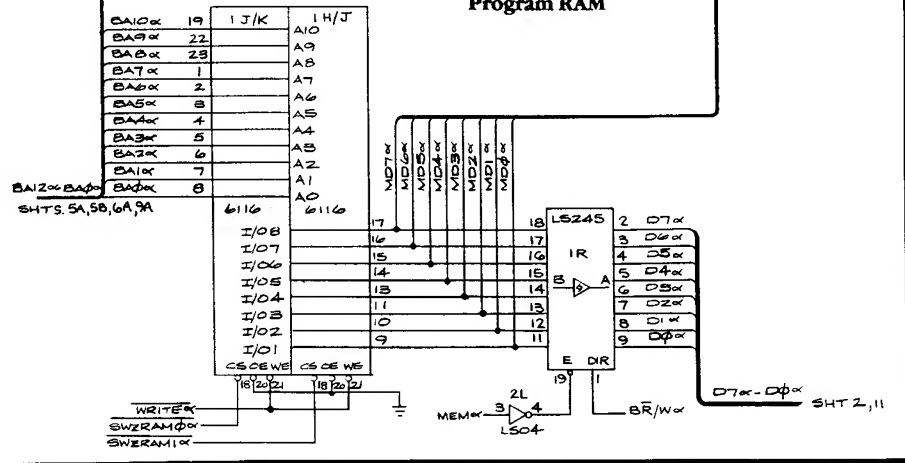


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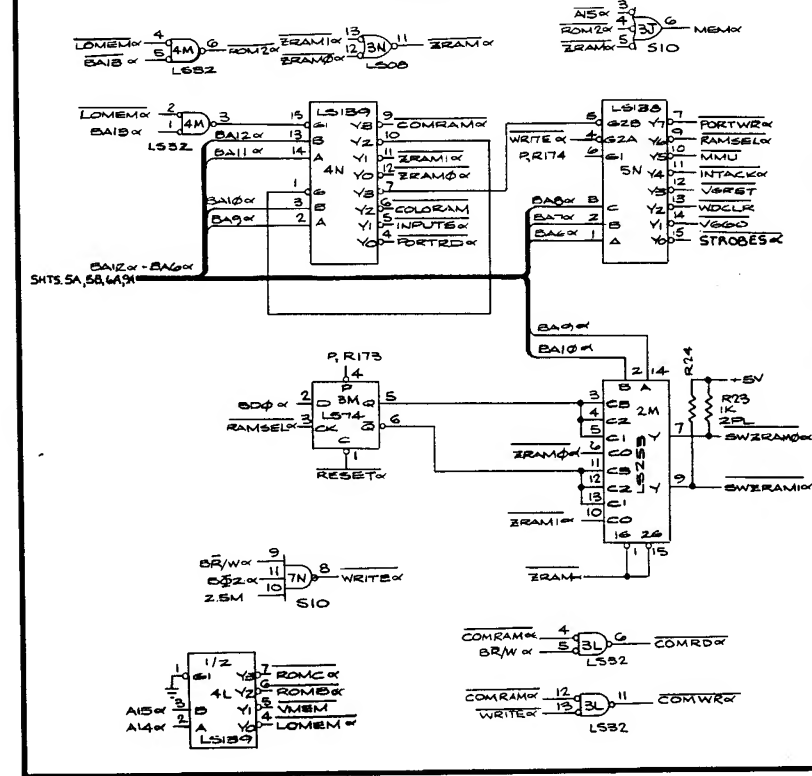
# Program ROM



# Program RAM



# Decoder



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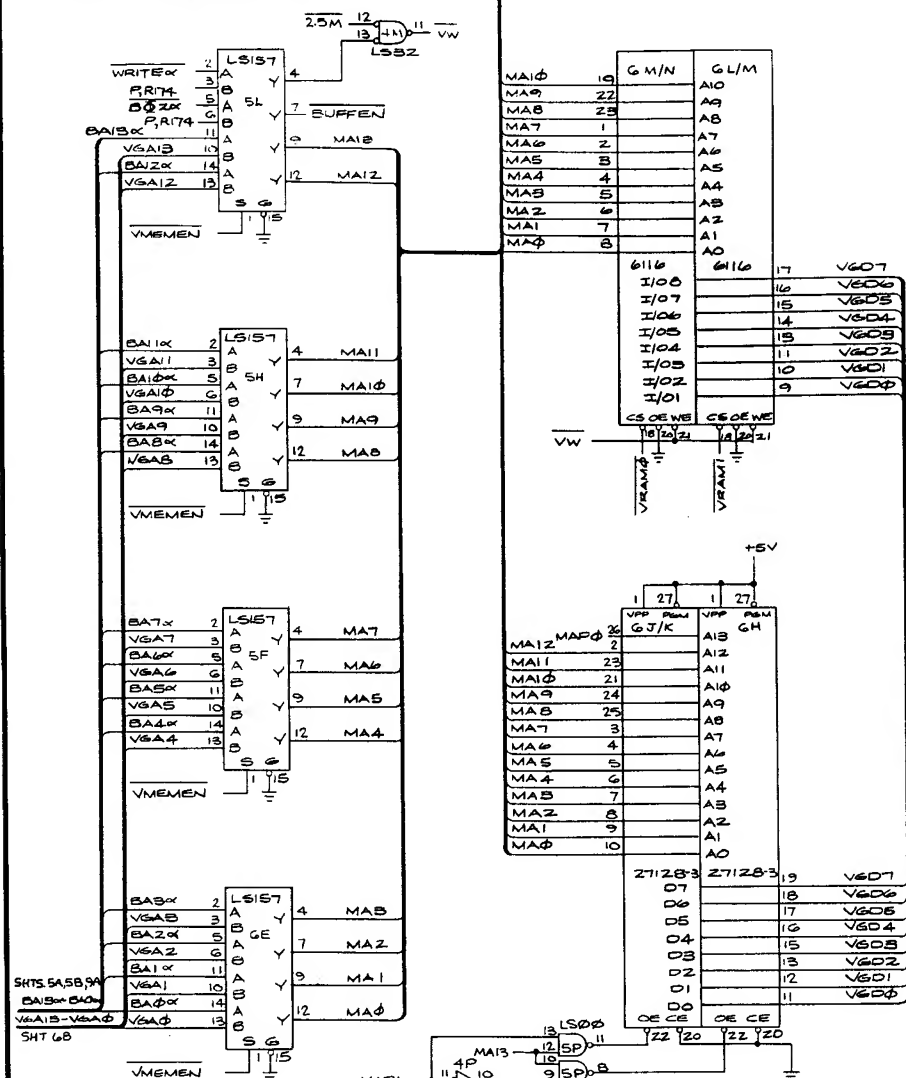
# MAJOR HAVOC Main PCB Schematic Diagram



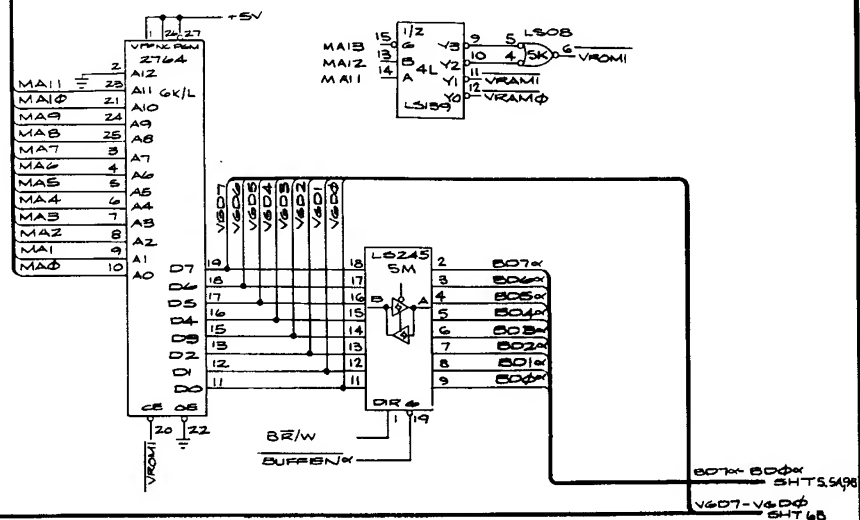
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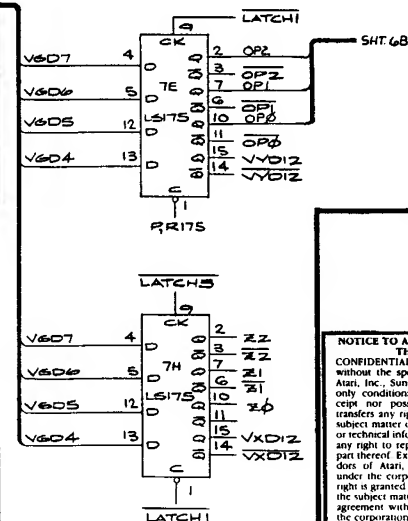
### Vector Generator Memory



МАИБ - МАФ 54768



### OP Code and Intensity Latches



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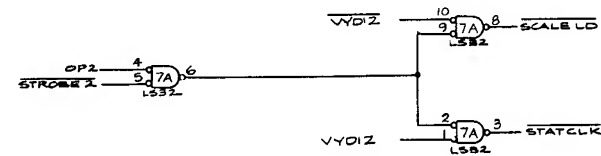
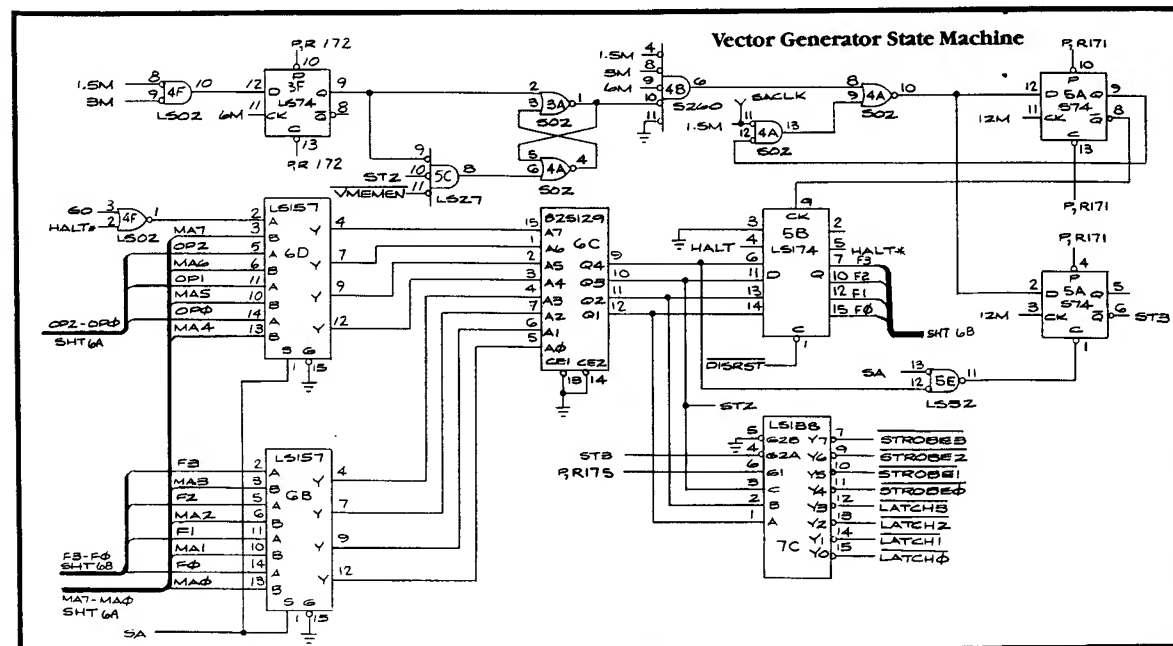
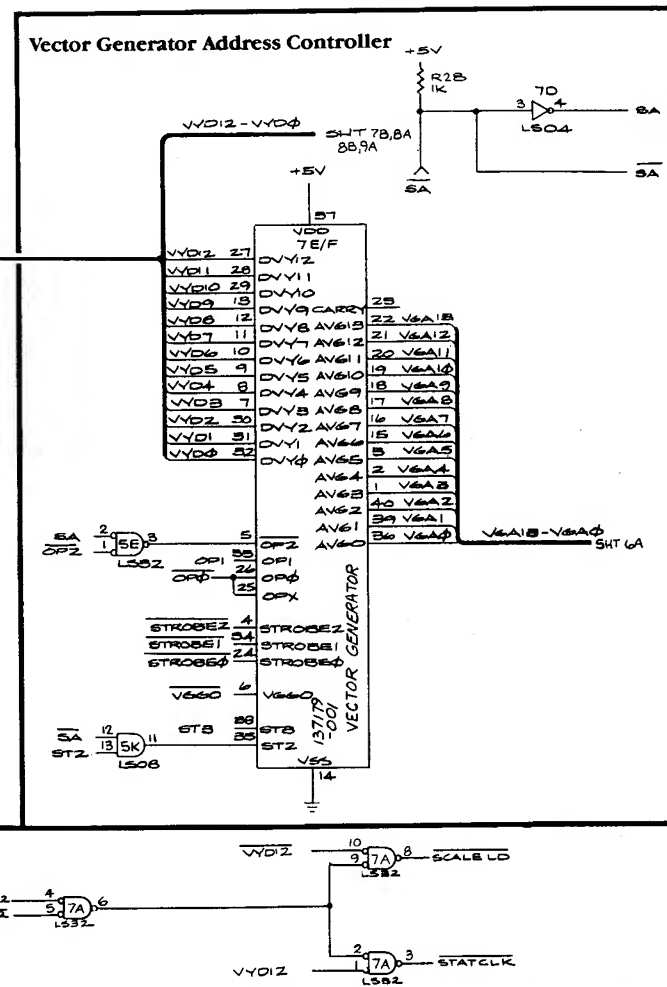
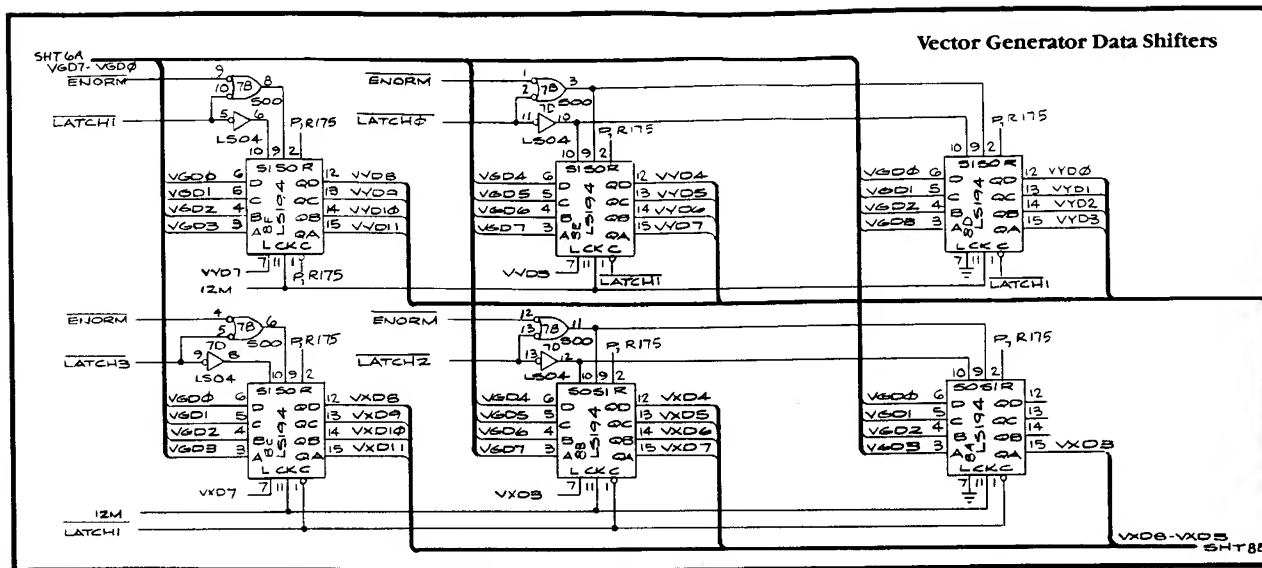
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### MAJOR HAVOC Main PCB Schematic Diagram



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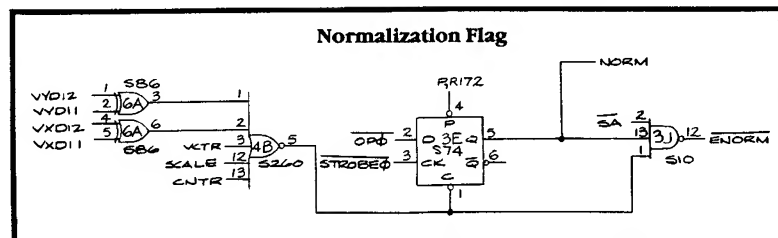
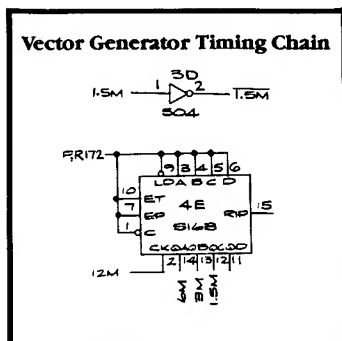
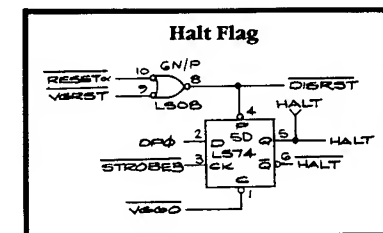
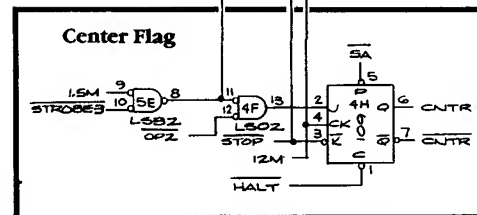
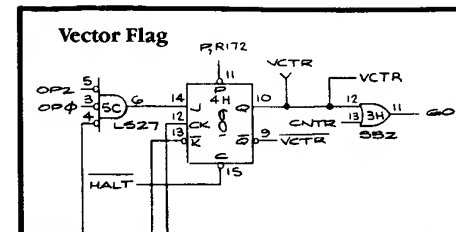
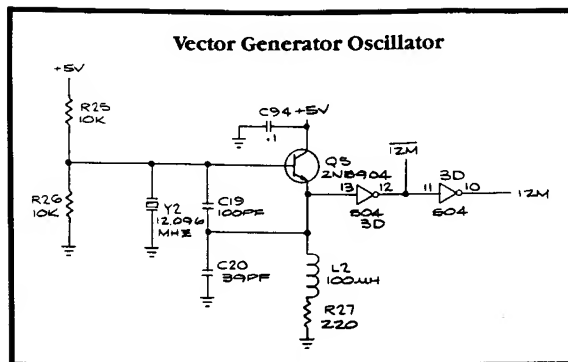
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### MAJOR HAVOC Main PCB Schematic Diagram



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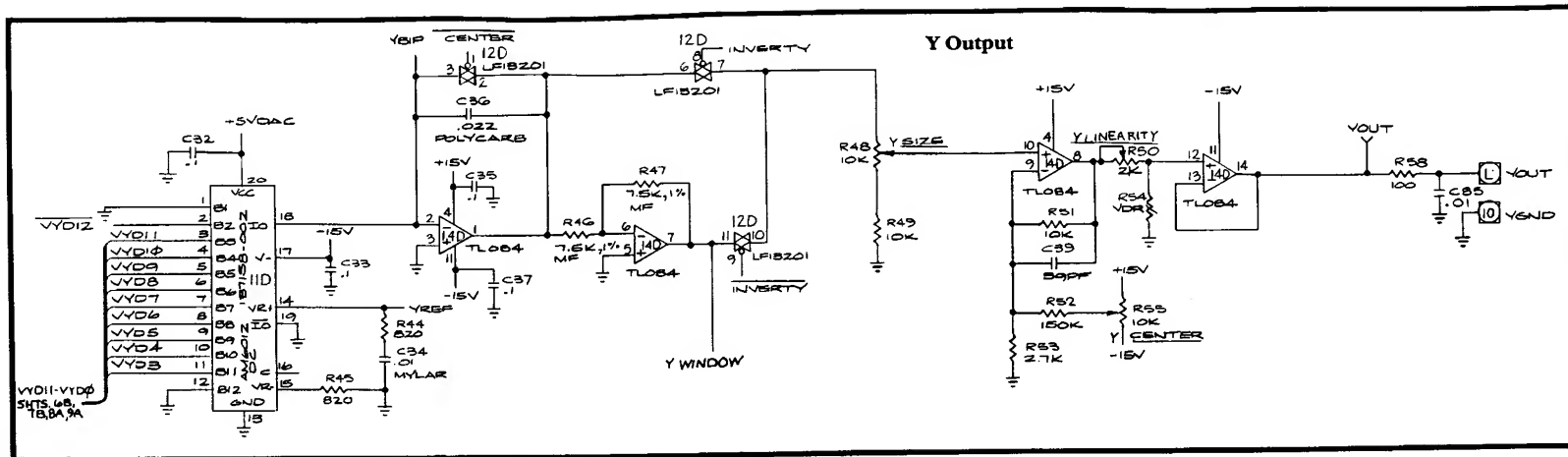
## MAJOR HAVOC Main PCB Schematic Diagram



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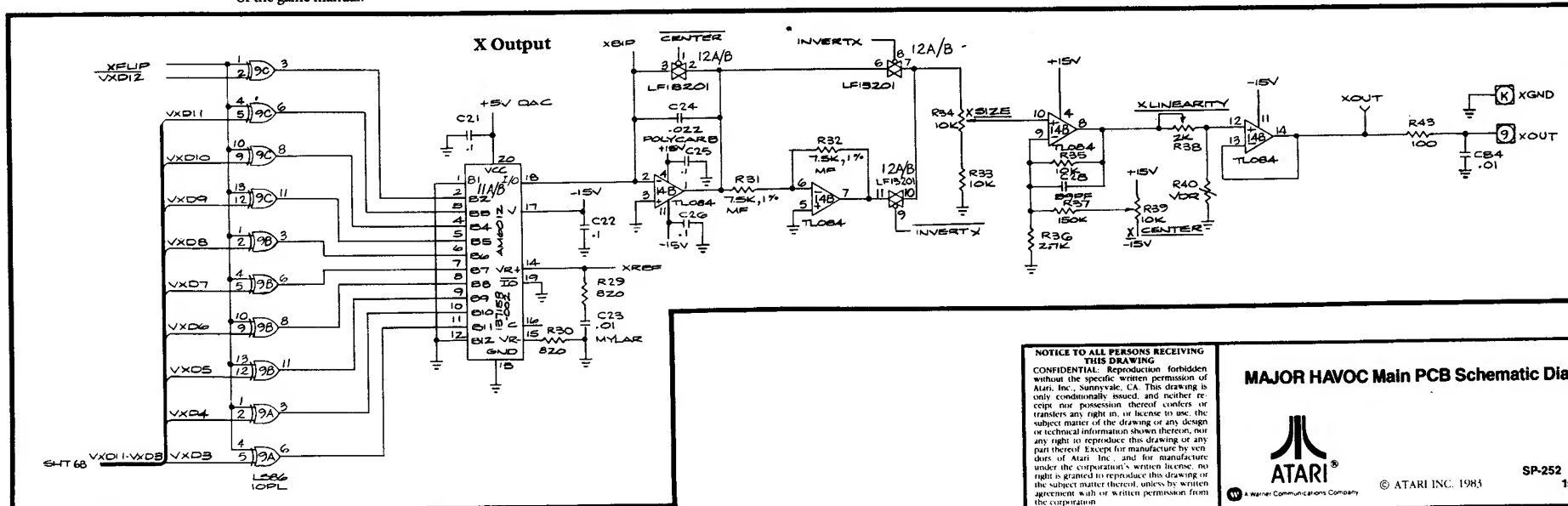




#### X and Y Video Adjustments

Perform the following procedure to adjust the display size, centering, and linearity:

1. Set the game to the SelfTest Mode and select the Crosshatch Pattern Display as described in Chapter 2 of the game manual.
2. Adjust XCENTER (R39) and YCENTER (R55) so that the crosshatch pattern is centered on the screen.
3. Adjust XSIZE (R34) and YSIZE (R48) so that all four corners of the red outline are off the screen and all four corners of the white outline are completely visible.
4. Adjust XLINEARITY (R38) and YLINEARITY (R50) so that the diagonal lines are straight and the diamond-shaped squares are symmetrical. Since the linearity potentiometers change the size of the display, it may be necessary to repeat step 3 to obtain the correct display.



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#### MAJOR HAVOC Main PCB Schematic Diagram



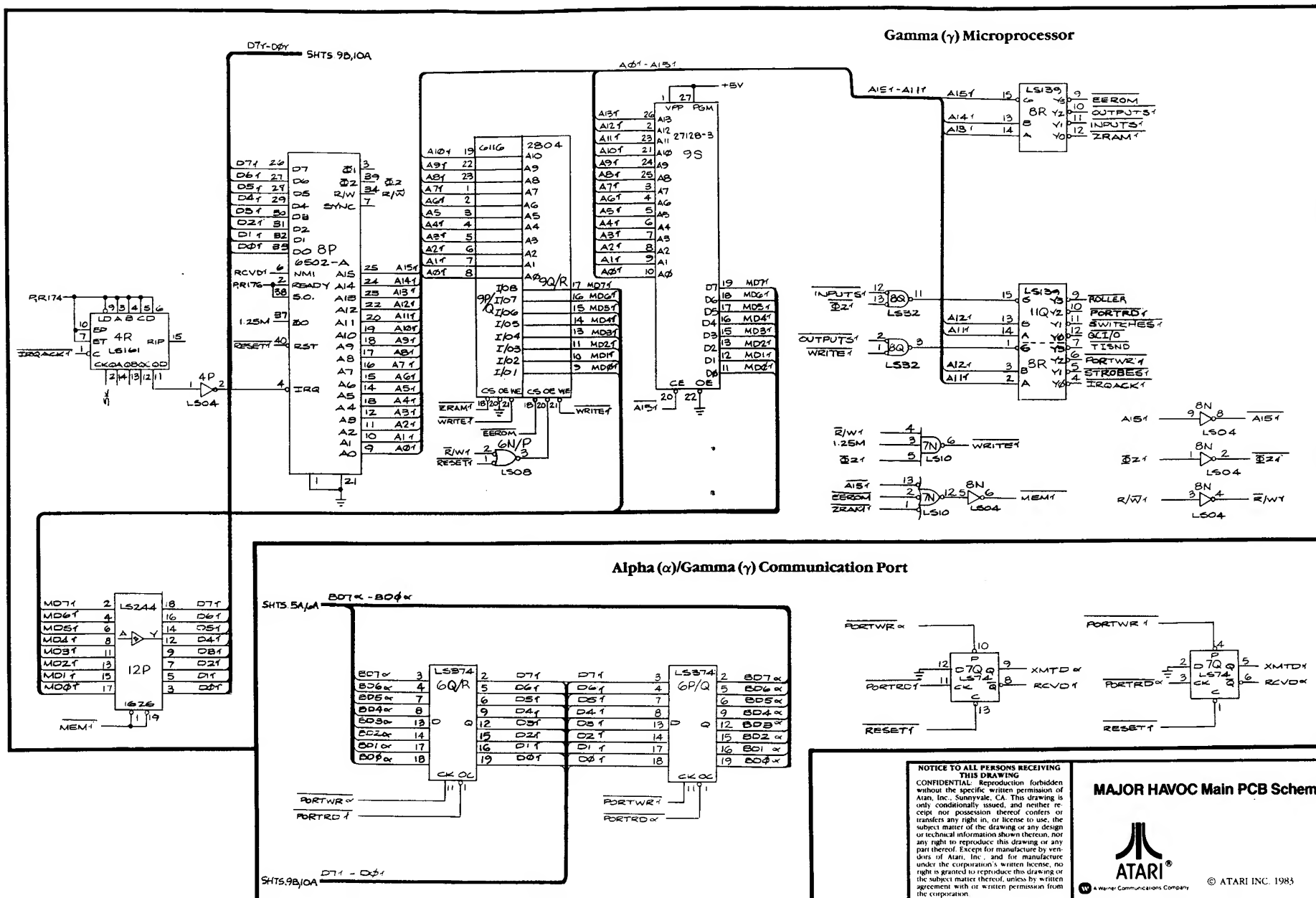
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1st printing

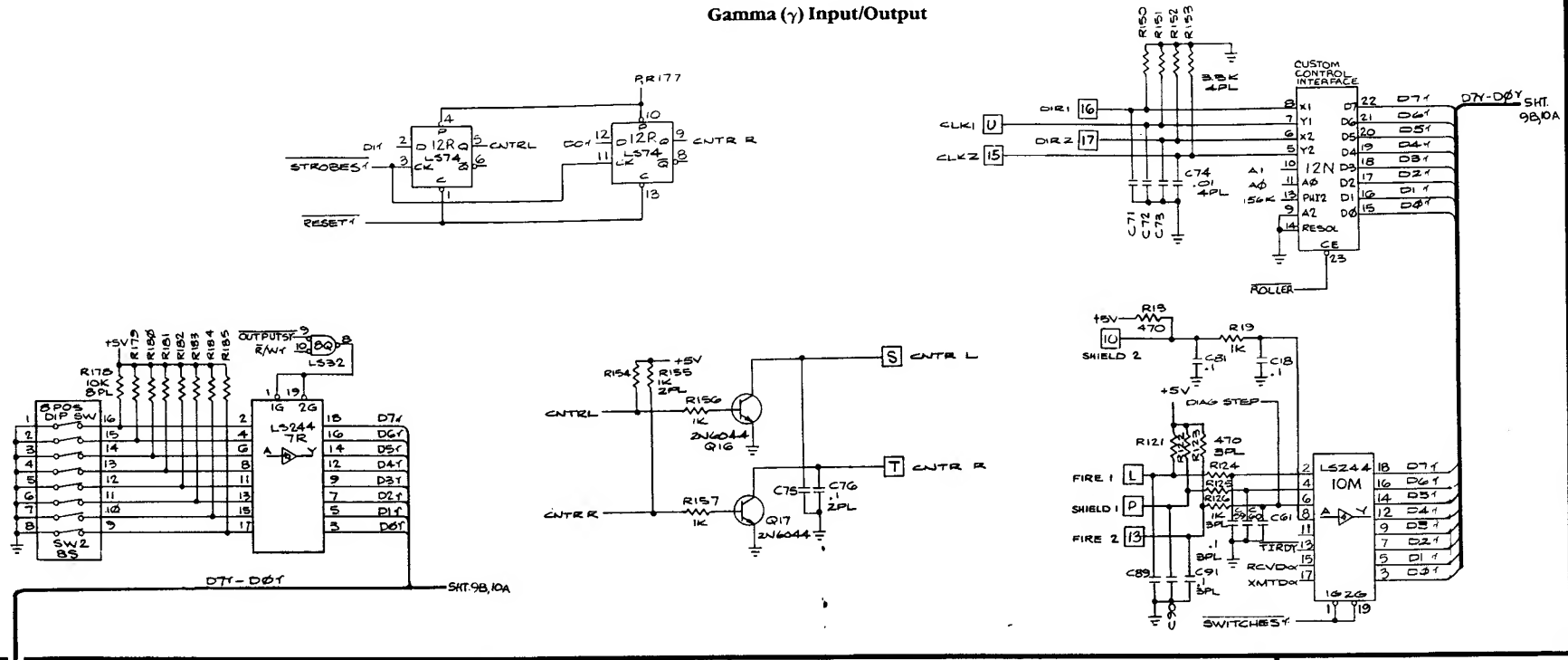




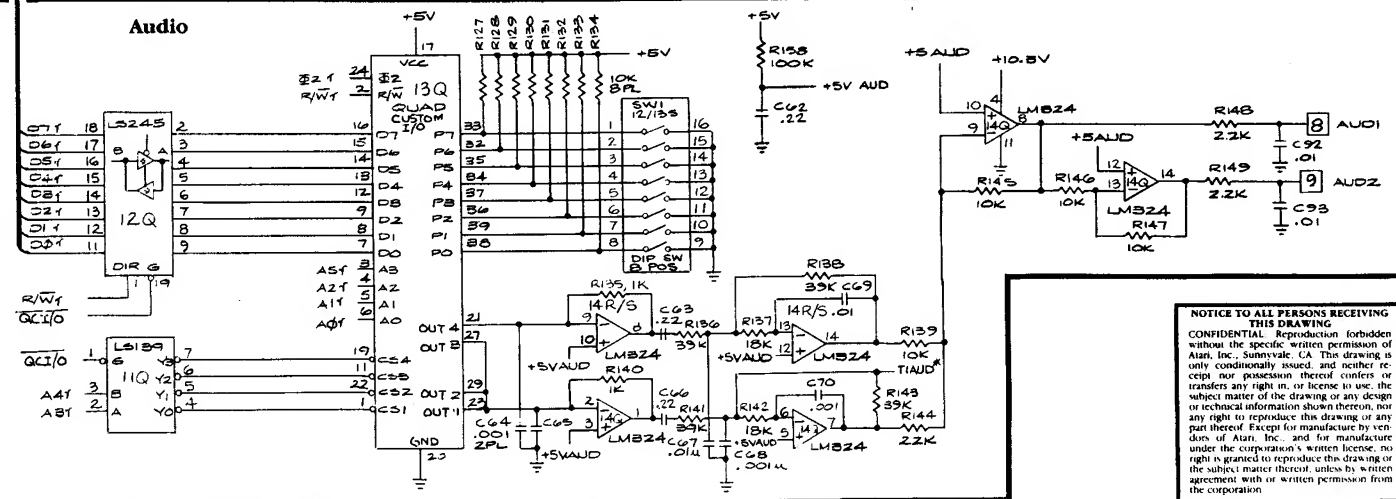




# Gamma (γ) Input/Output



## Audio



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## MAJOR HAVOC Main PCB Schematic Diagram



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